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# Design of Pulse-Triggered Flip-Flop

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*Abstract*—Low Power Flip-Flop design involves pulse triggered clock generation mechanism, in which explicit pulse triggering has several advantages. Among all detailed design methods, signal feed-through pulse triggered flip-flop is most effective in all design aspects, i.e., speed area and delay. In this paper, further modification of this design is suggested, along with FinFET based design is carried out, which further reduces the power dissipation inside the chip and optimizes PDP. All of the inventions are carried out using TSMC 30-nm design technology. HSPICE simulation software is used for waveform generation and power, timing parameter calculations.

*Keywords:* Explicit pulse triggered method, FinFET, Flip- Flop

## I. Introduction

Moore's law governs transistor count in Integrated Circuit (IC), and with the development of smaller devices, this count is increasing rapidly. As a result, power consumption inside a chip is enhanced, which aggravates the overall system's power requirement. At present most of the IC is digital, among which flip-flop is the pivotal element. It is responsible for the circuit's overall performance, functionality and timing attribute. Synchronous block consumes 30% to 60% of the device's total power, flip-flop and clock network consumes 90% of it. Thus reducing the power requirement for flops will reduce the overall system power budget. Timing parameters are strongly related to the system clock, so the clock tree's design is crucial. As a part of system power reduction, the clock's frequency can't be compromised, which will impede system performance. One way of reducing sufficient clock frequency is carried out by using a dual edge-triggered flip-flop. This flop samples data at both rising and falling clock edge and reduces system frequency by half. But dual-edge circuit has a different clock generation, which consumes a significant extra amount of power. As a remedy of power reduction, supply voltage can't be reduced below a certain level to avoid soft-error inside circuit nodes.[1],[2]

## II. Different P-FF and Modified Circuit Proposal

### A. Importance of Pulse-trigger Flip-Flop

Latch and Flip-flop are the primary storage elements in the digital synchronous circuit. Latch works on the voltage level of the clock signal, whereas flip-flop works on its edge. Latch provides a faster response with the help of time borrowing with lesser circuitry compared to flip-flop.[3] But it is susceptible to the glitches present at the data pin and causes higher dynamic power dissipation. To overcome the issue, the flip-flop is an effective solution. It rejects input glitches via sampling the data only at the clock edge (for the small duration). But it comes with a higher MOS count and extra power delay and area. Pulse trigger flop is the solution to all the problems as it takes advantages of both the device.

The idea behind the pulse triggered latch is to create a short duration pulse at the rising (or falling) edge of the system clock. The new derived pulse will drive the latch and sample data for this short duration. The pulse generation circuit and conventional latch structure will result in a positive edge trigger flip-flop. This design has many advantages over traditional master-slave architecture. By using time borrowing, principle pulse trigger flip-flop has lower D-to-Q delay and negative set up time.[4] The circuit will have a lesser area than a conventional flop as two stages are reduced to one. Precious control should be taken while designing the clock pulse as it will eventually create a window for data sampling. If the window is large, it will pass voltage spikes at data input to output, but if the pulse width is very narrow, it will not match with the device's speed and will not drive the latch. Due to the lower circuit count dynamic as well as static power dissipation of the circuit is reduced. Different techniques like Conditional recharge, Conditional Capture, and Conditional Pre-discharge methods are used along with pulse-triggered structure.[8-13] Above all, many statistical frameworks has been developed to optimize E-D (Energy Delay) graph and came out with a useful solution

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depending upon the application need( Performance critical, Energy Critical etc.) [6-7]

Depending upon the pulse generator, Pulse-triggered flip-flop can be subdivided into two types, implicit and explicit. Implicit type flip-flop (IP-FF)[8] has a build-in pulse generator circuit inside the flip-flop. Examples for this is hybrid latch flip-flop (HLFF)[10] , Semi-dynamic flip-flop(SDFF)[11] and implicit pulse data close to output(ip-DCO)[9]. Explicit type flip- flop(ep-FF) does not include the pulse generator inside flip- flop circuit, example explicit-pulsed data closed to output(ep- DCO) [9],etc. At first glance, the explicit pulse triggered flop to consume more power than the implicit pulsed triggered flip-flop. But ep-FF has some edge over the ip-FF. First, ep-FF can share it's clock generating circuit with adjacent FF, which is not feasible for ip-FF [13]. This makes it a more energy-efficient design. Dual-edge FF is easily compatible with ep-FF, which is not easy to design in ip-FF[23].

*B.* Different Types of Explicit flip-flop

*1)* ***Explicit Pulse Data Close to Output(ep-DCO)[9]****:*

With the help of a single-phase clocking and NAND gate-based pulse generator circuit, True-Single-Phase-Clock (TSPC) is generated in this circuit. This circuit is semi-dynamic in nature and fastest among other variants. I1-I2 and I3-I4 are inverter pairs used to hold data at the internal node (X) and an output node, respectively. When the clock is low X is pre-charged to high value and the output node is disconnected. When the clock rises to a high value due to the delay of three inverter AND gate procures a pulse, it opens M3 and M5 to capture the data. Based on the importance of input-output will be changed. This circuit has power dissipation as internal node charges and discharged every time along with the clock cycle when data is fixed. This repeated charging and discharging will cause glitches in output.

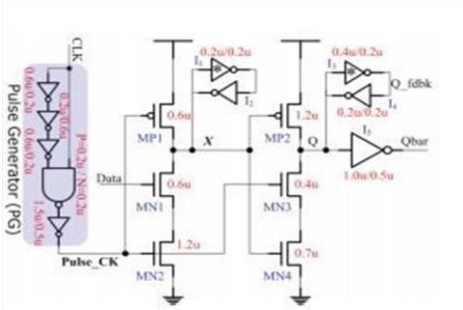


Fig. 1. ep-DCO

*1)* ***Conditional Discharge Flip-flop(CDFF)[9]****:* To solve unnecessary glitches in the internal node, the CDFF flip-flop is proposed. It implements Conditional Discharge logic in the discharge path [23] to stop the internal Node's excessive discharge. When data is high for a long time, Q fdbk is low, which eventually closes the discharge path. Internal Transistor pair I2 is replaced by week pull-up transistor Mp2.

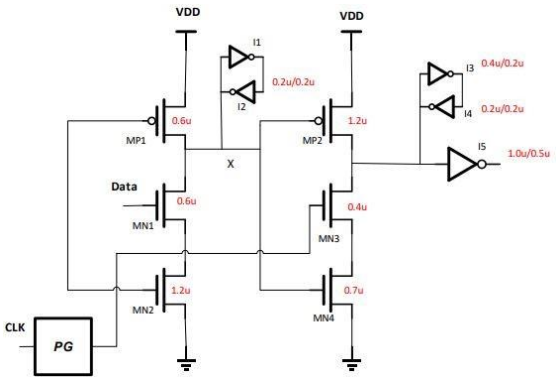


Fig. 2. CDFF

**3) Static-Conditional Discharge Flip-Flop(SCDFF)[9]:**

In the case of CDFF, the internal node's pre-charging is controlled by the clock signal, which makes the circuit dynamic in nature. To operate it in static mode, MP1 is connected to the data signal. Conditional discharge is controlled by Q fdbk signal, which is a complemented form of output. When the input is constantly high, Q fdbk is low, and it closes the discharging path as MN3 is in the cut-off. Also, due to the static inverter pair(I2, I3), internal node capacitance is low, making the circuit work faster. As the internal node charging is static, it reduces power dissipation by reducing switching activity for the internal node at the periodical interval.

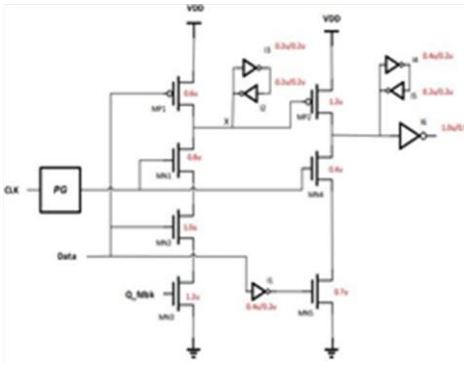


Fig. 3. Static-CDFF

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**4) Modified hybrid Latch flip-flop(MHLFF)[10]:**

To reduce the transistor count in the discharge path and glitches at the internal node, a modified hybrid latch flip-flop is proposed.

In this circuit, a transition occurs when data input is different in two consecutive clock periods. When the clock moves from low to high, depending on the delay associated with the inverter chain, short-duration Pulse CK is generated, and MN3 is On. If data(D) and output(Q) are the same, no change is observed at the output and internal nodes. But when D is low and Q is high, Internal node X is charged to high voltage via MP2, and Q is discharged via MN2-3. But if D is High and Q was low in the previous cycle, internal node X is discharged via MN1-3 path, which will open up MP1, and Q will be high. This circuit has some disadvantages. The pulse clock is driven by a voltage that is one threshold voltage lower than the supply voltage, it slows its operation. Another problem associated with the circuit is when both D and Q are low internal nodes floating, which causes high power dissipation.

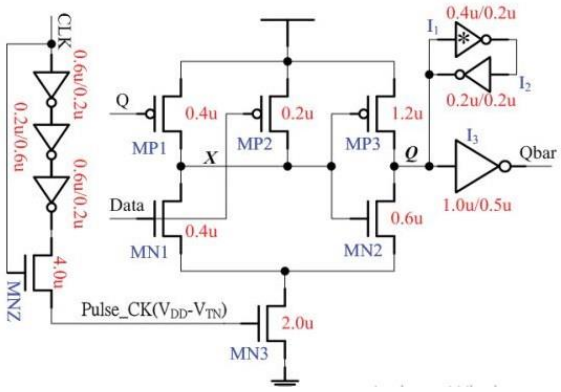


Fig. 4. MHLFF

**5) Signal Feed through Flip-flop(SFTFF):** All of the circuits mentioned above have unequal rise and fall time delay, which leads to a lower duty ratio at the output. This circuit resolves this problem. SFTFF is better in terms of speed and power budget. It involves the fundamental operating principle of SCDFF, eliminating unwanted switching activity at an internal node and eliminating power dissipation. This circuit has some significant structural difference compared to previous circuits. A week-pull up pseudo-p-MOS transistor MP1 is used, which helps in eliminating the keeper circuit at an internal node.[13] [14] The Next change is the use of pass transistor MNX controlled by pulsed clock, connected to the output node Q. This scheme is also known as signal feed-through. This pass transistor has a dual role of feeding signal at output node and providing a path for output node to discharge. As discharging is done via pass transistor, the pull-down network is removed.

The principle of operation of the circuit is discussed below. In the presence of clock pulse, when there is no transition in the data signal, i.e. data input is the same as output, no current will flow through MNX and this will reduce driving effect at the input node. At the same time as Data and Q fdbk are complementary in nature the discharge path through MN1-3 is closed. This also reduces signal switching at the internal node X. When there is "0" to "1" transition, the internal node is discharged through MN13 and this makes MP2 on and output node is connected to high voltage. There is another path through MNX, which connects high data input to the output node. Both of the processes complement each other and speeds up charging of output node. When data transition occurs from "1" to "0" MNX conducts for a shorter duration and the output node is discharged through pass transistor MNX. Since MNX is turning on for a shorter period, the input node's loading effect is not that severe. In this circuit both charging and discharging is done via MNX, this reduces the overall delay of the system while maintaining equal rise and fall time delay. This circuit is better in all three aspects of design,i.e speed area, and power.

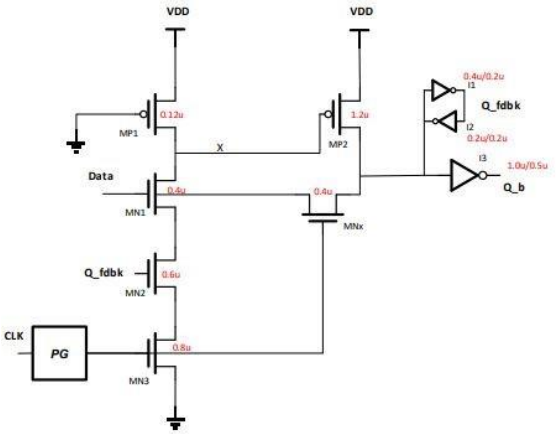


Fig. 5. SFT

**6) Modified Signal Feed through Flip-flop (SFTFF)**: pseudo-n MOS in SFTFF dissipates power throughout its operation irrespective of the input andoutput value. This causes significant increase in overall power dissipation inside the chip. To prevent this, modified device uses data pin to connect the gate terminal. Now depending on the value of input , pMOS is on and which reduces overall power dissipation across it. Operation of the circuit is similar to the SFTFF. When there is no change in data for consecutive clock periods there will be no loading effect on the input node. When there is "1" to "0" transition output node is charged via pass transistor as well as via MP2. When there is "0" to "1" transition output node is discharged via pass transistor. Output node is modified as one of the inverter in keeper circuit is changed with week pull-up transistor MP3.

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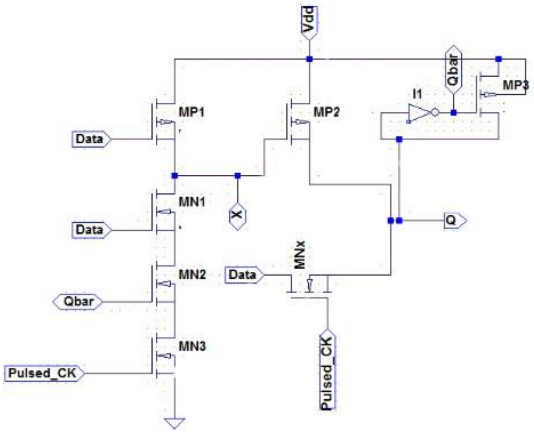



Fig. 6. Proposed-SFTFF

**7) Modified Signal Feed through Flip-flop (SFTFF)** Design using FinFET: As discussed earlier, modified signal feed through the flip-flop is best among all the designs developed earlier. With the advancement of technology, device size is reducing significantly. Short channel effects, sub-threshold leakage, and gate oxide tunnelling also increase in shorter channel devices, making higher off-state current. FinFET provides solutions below 22nm technology. FinFET is a quasi- planner Field-effect transistor with similar functionality as conventional MOS, but there is a structural difference. Channel( length is Lg ) is perpendicular to the bulk of MOS. These channels are also known as FIN. Gate oxide thickness Tsi is patterned on top of the channel. The device's effective width is 2nTfin, where n is the number of FINS(NFINS) and Hfin is the height of the FIN, and these two are device parameters. So depending on the parameter value, channel width is quantized in FinFET. Two other parameters are NRS (Square of Source Diffusion) and NRD(Square of Drain Diffusion).[20-22]. So based on the parametric values, the device W/L ratio changes and all terminal characteristics are modified.

## III. SIMULATION RESULTS

All of the designs was first carried out using TSMC 90 nm technology file. 90nm file design shows glitch in output at the beginning of the output. 30nm FIFET based design solves this. Along with that FinFET provides higher speed and low leakage power in comparison with other variants. Also it is noted that the output node is connected with 20-fF Capacitor and an extra loading capacitor 3fF is used. HSPICE is used for simulation. Operating condition is 500MHz/1.0V [10-12].

### A. Timing Diagram

In all the timing diagrams system clock is the conventional clock generated by PLL . Pulsed clock is generated using pulse triggered circuit. Output follows data signal at rising edge of the clock. In case of MHLFF,Pulsed clock is not properly generated, because the driving voltage is low(one threshold voltage lower than supply) and makes pulse generated circuit response slower.

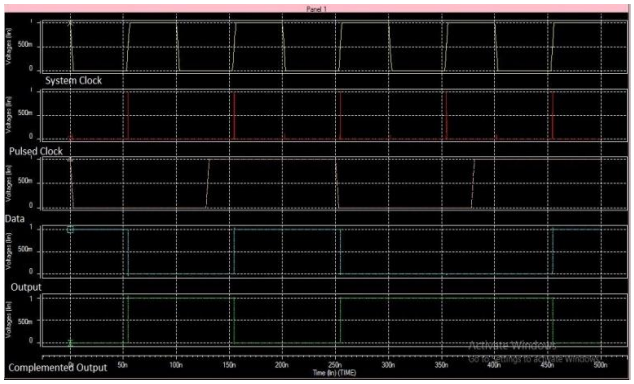
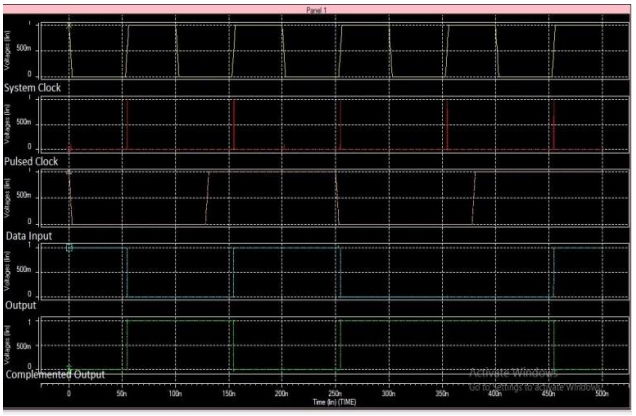



Fig. 7. ip-eco Waveform




| FF Type | Ep-DCO | CDFF | SCDFF | Ep-SFF | SFTPFF | Proposed SFTPFF | FinFET |
|---|---|---|---|---|---|---|---|
| (Clk,Data)=(0,0) | 52.47 | 53.77 | 59.05 | 48.71 | 52.43 | 50.41 | 7.42 |
| (Clk,Data)=(0,1) | 58.91 | 51.25 | 52.09 | 54.86 | 52.77 | 53.11 | 8.11 |
| (Clk,Data)=(1,0) | 58.99 | 59.26 | 65.26 | 61.79 | 59.03 | 58.89 | 11.12 |
| (Clk,Data)=(1,1) | 66.67 | 68.12 | 74.69 | 71.23 | 70.33 | 71.11 | 15.12 |
| Average | 59.26 | 58.1 | 62.77 | 59.14 | 58.62 | 58.38 | 10.4425 |

Fig. 9. SCDFF Waveform

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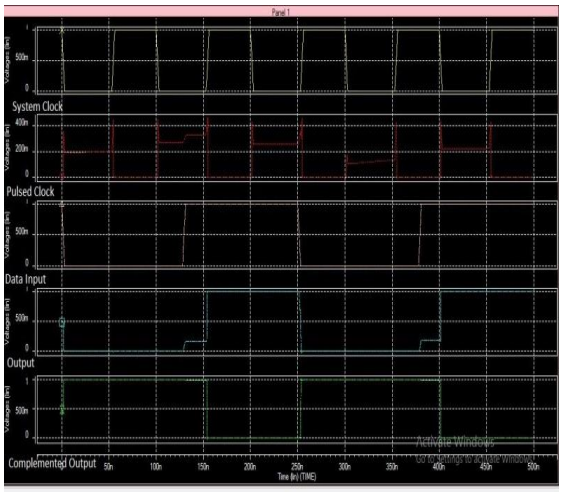


Fig. 10. MHFF Waveform

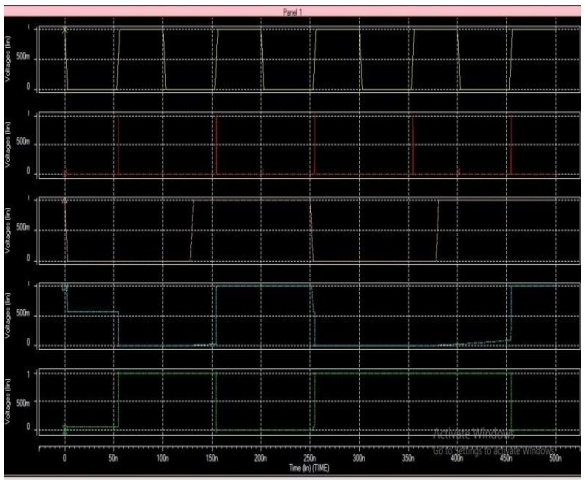

Fig. 11. SFTFF Waveform

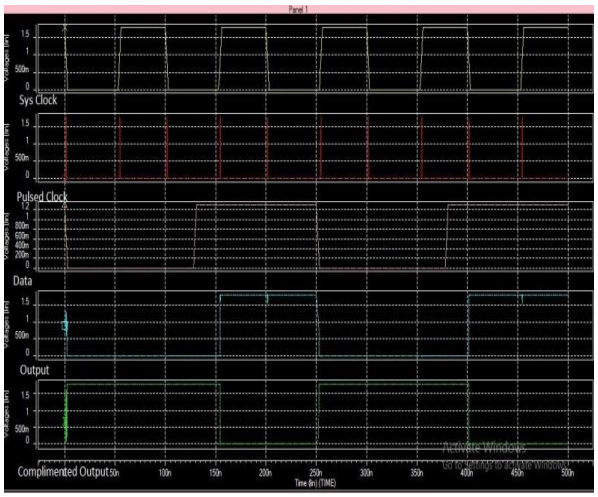


Fig. 12. Modified SFTFF Waveform

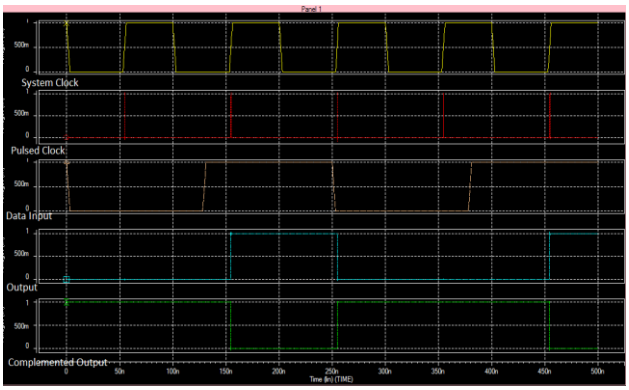


Fig. 13. Modified SFTFF(FinFET) Waveform

| FF Designs | ep-DCO | CDFF | SCDFF | MHLFF | SFTPFF | Modified SFTPFF | FinFET SFTPFF |
|---|---|---|---|---|---|---|---|
| Number of transistors | 28 | 30 | 31 | 19 | 24 | 23 | 23 |
| Average Power(1 Cycle) in µW | 24.84 | 31.91 | 24.18 | 15.05 | 23.46 | 22.41 | 0.34 |
| Average Power(2 Cycle) µW | 25.81 | 32.23 | 25.43 | 18.33 | 24.31 | 24.3 | 0.36 |
| Average Power(3 Cycle) in µW | 28.67 | 33.04 | 29.39 | 23.41 | 27.66 | 27.61 | 0.39 |
| Average power (0% all-1) µW | 23.92 | 20.5 | 20.94 | 14.28 | 19.49 | 20.01 | 0.43 |
| Average power (0% all-0) µW | 20.31 | 19.95 | 20.31 | 12.26 | 18.21 | 14.11 | 0.391 |
| Average Power | 24.71 | 27.526 | 24.05 | 16.666 | 22.626 | 21.688 | 4.9822 |
| Delay (µs) | 0.20046 | 0.20052 | 0.20057 | 0.325 | 0.2005 | 0.2 | 0.2 |
| PDP(pJ) | 4.9533666 | 5.51951352 | 4.8237085 | 5.41645 | 4.536513 | 4.3376 | 0.99644 |
| EDP(attoJ-s) | 0.992951869 | 1.106772851 | 0.967491214 | 1.76034625 | 0.909570857 | 0.86752 | 0.199288 |
| Setup Time(ps) | -83.4 | -87.9 | -44.8 | 1.2 | -85.6 | -85.5 | -84 |
| Hold Time(ps) | 111 | 122.56 | 122.6 | 94.7 | 120 | 120.02 | 121 |

Fig. 14. Timing and Power Feature comparison of different Flops

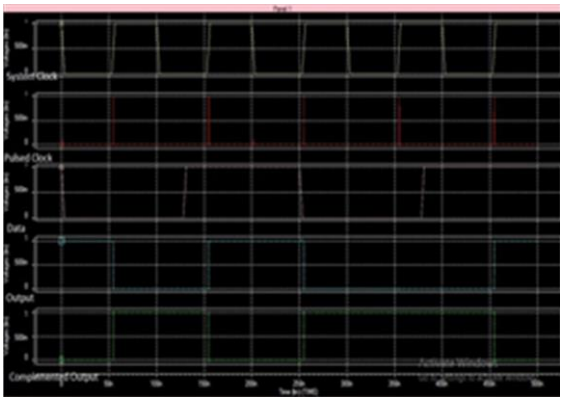

Fig. 15. Leakage Power Consumption in Standby Mode(nW)

**B. Power Consumption of FF Designs**

Figures 14 and 15 summarizes all Power, area, and timing related attributes for all the flip-flops. As per area is a concern, the proposed design is not optimized in terms of the number of flops, but it has the lowest layout area. Power dissipation is of two types dynamic and static. In the case of dynamic power dissipation, a 500 ns time frame is

selected as a reference. Within this time, one, two, and three data switching activities are taken into consideration. Power dissipation is tabulated; two other cases have been considered; the first case, the input is high throughout this time frame as high another case zero. In the case of static power dissipation depending upon four combinations of data and clock power dissipation is captured. FinFET based modified SFTFF is the most power economical for both static and dynamic cases.

### *C.* Timing Parameters of FF Designs

Timing parameters are Data to Output Delay(D-to-Q), setup and hold time. Data to output delay measures the speed of the system. It is the average of the rise and fall time delay. Setup time is the minimum time before the clock edge when data must be stable. In other words, it is the optimal time of data to be applied for minimizing the product of power and delay. (PDP). All the cases except MHLFF have a negative setup time due to a delay in the clock pulse generating circuit. With this setup, time information holds time when the slope of Clock-to-Q delay vs Hold time is -1. One of the critical parameters is PDP and the main aim is to minimize this. Modified design, as well as FinFET is the most optimized design among all the cases.

## III. CONCLUSION

Static Signal Feed-through Flip-Flop is most effective in terms of area, speed, and delay. Signal feed through mechanism is the key technique by which equal rise and fall time delay is maintained. pseudo-pMOS logic has been replaced by applying a data signal at the node to reduce more static power. Using FinFET PDP is optimized and it is the most performance efficient design mechanism.

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