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A Novel Sense Amplifier Design for Efficient Memory Read Operation

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Abstract - Sense amplifier is one of the most important critical circuit in the periphery of CMOS memory array structure. It plays an important role in memory (SRAM and DRAM) read operation. The memory access time and overall memory power dissipation is greatly affected by the performance of sense amplifier. A novel 9T sense amplifier architecture is proposed in this paper which operates with less delay and low power. The sense amplifier proposed in the paper operates in two modes. In precharge mode the outputs get precharged to full supply voltage and in sensing mode sense amplifier comes to active state by enabling sense input. In sensing mode sense amplifier senses the output of the SRAM cell correctly during its read operation. Design metrics such as dynamic power, delay and power delay product, energy and energy delay product are taken into account. All the sense amplifiers were designed using SYNOPSYS EDA tool and simulated in 30nm technology. Simulation results shows that the proposed sense amplifier provides better performance than other conventional sense amplifiers.

Keywords SRAM, sense amplifier, precharge mode, sensing mode, delay, energy.

I. INTRODUCTION

Memories (SRAM) occupy more than seventy percentage of System on chip (SOC) area so SRAM's power, delay, area and leakage are significant factors to be considered in performance of SOC. CMOS memories are required to increase speed, improve capacity and maintain low power dissipation in today's IC which defined a new operating environment for future sense amplifier. These objectives are conflicting when it comes to sense amplifier design [2]. The bit line parasitic capacitance increases with increase in memory capacity. The voltage sensing and bit line voltage swing slows down with increased bit line capacitance which results in energy hungry memories. As the size of the memory is decreasing and the storing capacity is increasing in the present day scenario the time response for the data writing and reading from the memory should be very fast [1]. In memory devices, large capacitive loads cause a major sensing delay so high speed sense amplification for memory cell signals is the key to achieve a fast access time in SRAM.

The memory array structure [14] consisting of memory unit, sense amplifier, control unit, row and column decoder is shown in Fig. 1. The sense amplifier is an active circuit that reduces the time of signal propagation from accessed memory cell array.

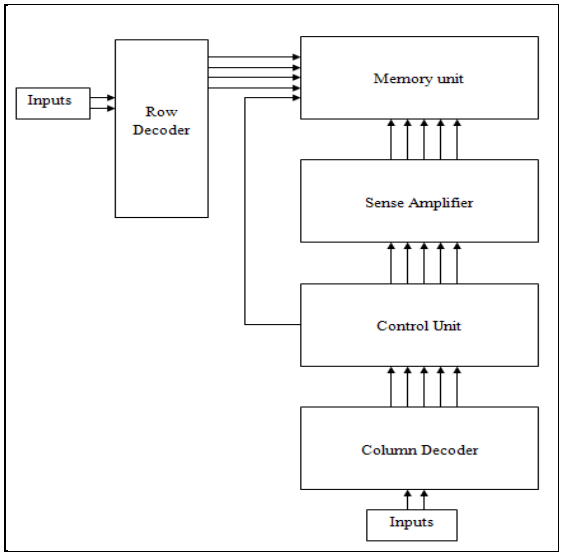

Fig. 1 Memory array structure

The circuit design of different sense amplifier types and other substantial elements of sense circuits is necessary to be understood to improve the speed, performance of memory and to provide signals which confirm the requirements of driving

peripheral circuits within the memory. The main function of the sense amplifier [3] is to sense or detect the data from the selected memory cell. The sense amplifier first senses the voltage from a bit line which represents a data bit (1 or 0) stored in a memory cell and then amplify the small voltage swing to recognizable logic levels. Each column of cells within the SRAM array requires only one sense amplifier [6] since only one row of data is accessed during each read cycle. On a digital memory chip it is the only analog circuits. Sometimes there occurs undesired data output while reading the data in the memory if the sense amplifier is not designed properly.

Sense amplifier works in two modes. Precharge mode occurs before each read cycle the bit lines are precharged to ensure that the difference between the bit line voltages are caused by the value that is stored in the cell [5]. There is a chance that the sense amplifier could misread and present an incorrect value at the output, if the bit lines are not precharged. In sensing mode, sense amplifier works by sensing a relatively small difference between the voltages of the two bit lines, then amplifying the difference at the output to show whether a cell is storing either a logic 1 or 0. To ensure full logic level at the output often times sense amplifiers are followed by an output buffer.

Sense amplifier is classified based on the circuit types and operation modes. Based on the circuit type sense amplifier is classified into two, differential and non differential. Differential sense amplifier is mostly preferred as it distinguishes smaller signals from noise and also starts signal detection sooner than the another one. The main drawback of differential sense amplifier is increase in area over non differential. Based on the circuit types sense amplifier is classified into three

1. Voltage sense amplifier: As name specifies, sense amplifier which detects the voltage difference on the bit lines is called voltage mode sense amplifier. It detects the low voltage level signal from the bit lines and produce a high swing signal as an output [4]. A small voltage swing appears on the bit line, when the cell is in read mode which is further amplified by differential couple and use to drive digital logic. The drawbacks of this sense amplifier are bit line voltage swing is becoming smaller and reaching the same magnitude as bit line noise. This sense amplifier is not the perfect choice where the time is primary concern because the delay of the voltage mode sense amplifier increases as increases of the capacitances.

2. Current sense amplifier: This amplifier is used to detect the current difference between the bit lines to determine whether a '1' or '0' is stored in the memory cell. The amplifier directly measures the cell read current and transfers it to the output circuits. The advantages of this approach is it can overcome the restriction of gain reduction brought on by voltage mode sense amplifier at low power supply voltage [2]. This amplifier has small input and output impedance which results in reduction in sense circuit delay, substrate current and substrate voltage modulation.

3. Charge transfer sense amplifier: The operation of this amplifier is based on the charge redistribution mechanism between very high bitline capacitance and low output capacitance of sense amplifier [4]. The advantage of this amplifier is, due to high bitline capacitance it provides low power operation without sacrificing speed.

Performance metrics to be considered during the design of sense amplifier [9]
1. Minimum sensing delay
2. Minimum power consumption
3. Maximum voltage swing
4. High reliability
5. Optimized layout area
6. Specified environmental tolerance

The rest of paper is organized as follows. Section 2 presents different conventional sense amplifier design. Section 3 describes working of proposed sense amplifier. Section 4 presents simulation results and graphical analysis. Section 5 concludes the paper.

II. DESIGN OF CONVENTIONAL SENSE AMPLIFIERS

In this section we review some existing sense amplifier designs which were designed to sense or detect the data stored in the memory during read operation.

A. Conventional Sense Amplifier Designs

2.1 Positive Feedback Differential Voltage Sense Amplifier (PFDVSA)

The PFDVSA consists of seven transistors in which one transistor is used to precharge the output nodes [12] of sense amplifier and two transistors are enabled for sensing the data at the output. The schematic diagram of PFDVSA is shown in Fig. 2

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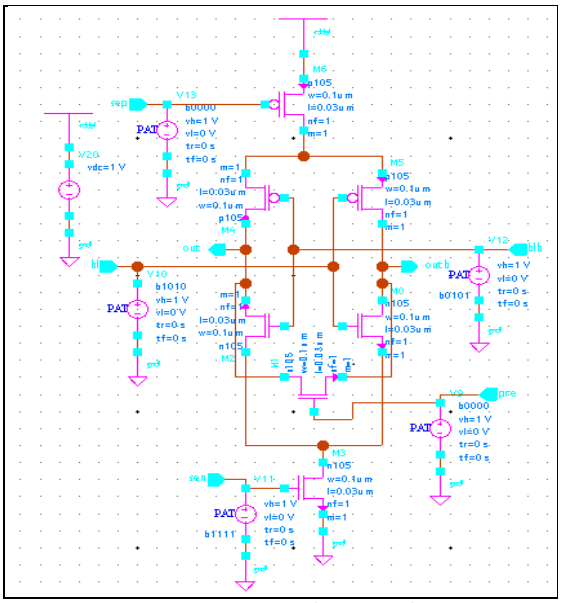

Fig.2 Schematic diagram of positive feedback differential voltage sense amplifier

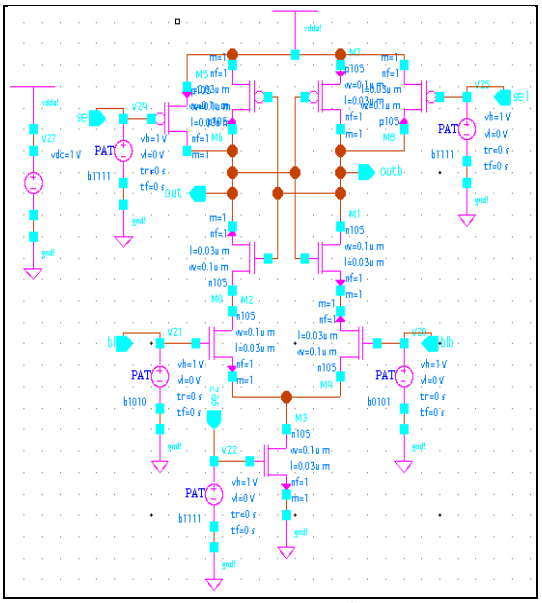

Fig.3 Schematic diagram of latch type sense amplifier

The sense amplifier operates in two modes, precharge mode and sensing mode based on the values of control signals "sep", "sen" and "pre". During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M1 transistor is made ON by enabling the control signal "pre". During precharge mode other control signals are given values such that they are disabled ("sen"=0, "sep"=1). During sensing mode control signals "pre" is disabled and "sen" and "sep" are enabled so M3 and M6 transistors are turned ON, which allows supply voltage and ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb".

2.2 Latch Type Sense Amplifier (LTSA)

The LTSA consists of nine transistors in which two transistors [5] are used to precharge the output nodes of sense amplifier and one transistor is enabled for sensing the data at the output. The schematic diagram of LTSA is shown in Fig. 3

The sense amplifier operates in two modes precharge mode and sensing mode based on the values of control signals "se", "se1" and "se2". During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M5 and M8 transistors are made ON by enabling the control signal "se" and "se1". During precharge mode other control signal "se2" is disabled. During sensing mode control signal "se2" is enabled and other control signals are disabled so M3 transistor is turned ON which allows ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb". In case if the inputs are not available during sensing mode the precharged value acts as an input for that particular time period.

2.3 Conventional Current Mode Sense Amplifier (CCMSA)

The CCMSA consists of twelve transistors in which three transistors are used to precharge the output nodes [8] of sense amplifier and one transistor is enabled for sensing the data at the output. The schematic diagram of CCMSA is shown in Fig. 4

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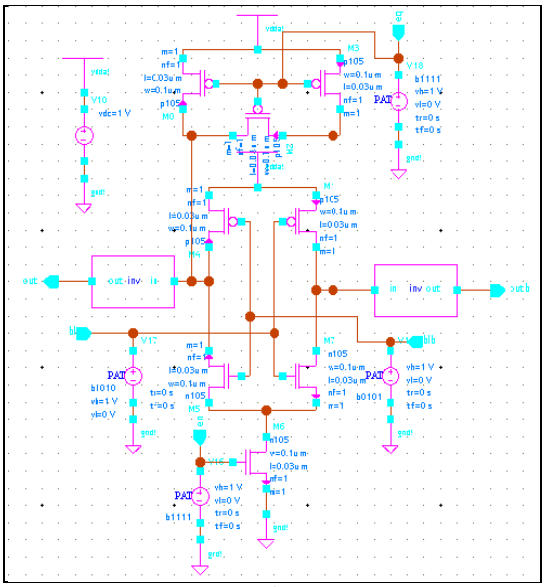

Fig. 4 Schematic diagram of conventional current mode sense amplifier

The sense amplifier operates in two modes precharge mode and sensing mode based on the values of control signals "eq" and "en". During precharge mode the output nodes "out" and "outb" are kept at zero volt as M0, M2 and M3 transistors are made ON by enabling the control signal "eq". During precharge mode other control signal "en" is disabled. During sensing mode control signals "en" is enabled and "eq" is disabled so M6 transistor is turned ON which allows ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb" .

2.4 Alpha Latch Sense Amplifier (ALSA)

The ALSA consists of twelve transistors [10] in which one transistor is used to precharge the output nodes of sense amplifier and one transistor is enabled for sensing the data at the output. The schematic diagram of ALSA is shown in Fig. 5

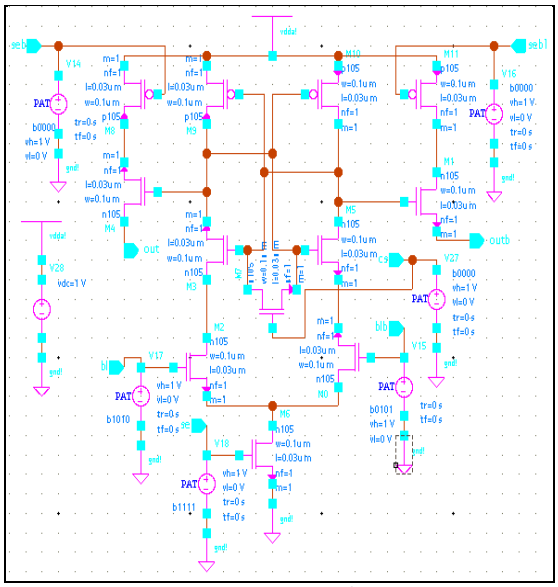

Fig. 5 Schematic diagram of alpha latch sense amplifier

Based on the values of control signals "cs", "se" and "seb", the sense amplifier operates in two modes precharge mode and sensing mode. During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M7 transistor is made ON by enabling the control signal "cs". During precharge mode other control signal "se" and "seb" are disabled. During sensing mode control signals "se" and "seb" are given 1 and 0 so M8, M11 and M6 transistors are turned ON which allows supply voltage and ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb". In case if the inputs are not available during sensing mode the precharged value acts as an input for that particular time period.

2.5 Decoupled Latch Sense Amplifier (DLSA)

The DLSA consists of twelve transistors in which one transistor is used to precharge the output nodes of sense amplifier and one transistor is enabled for sensing the data [7]. In DLSA inputs are provided to the amplifier only during sensing mode which is the main difference between ALSA and DLSA. The schematic diagram of DLSA is shown in Fig. 6

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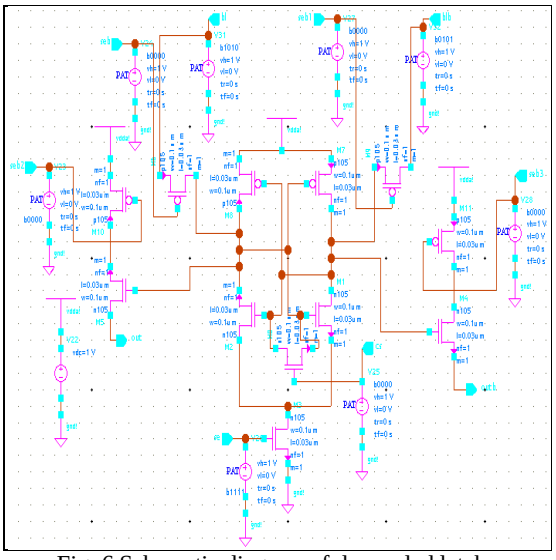

Fig. 6 Schematic diagram of decoupled latch sense amplifier

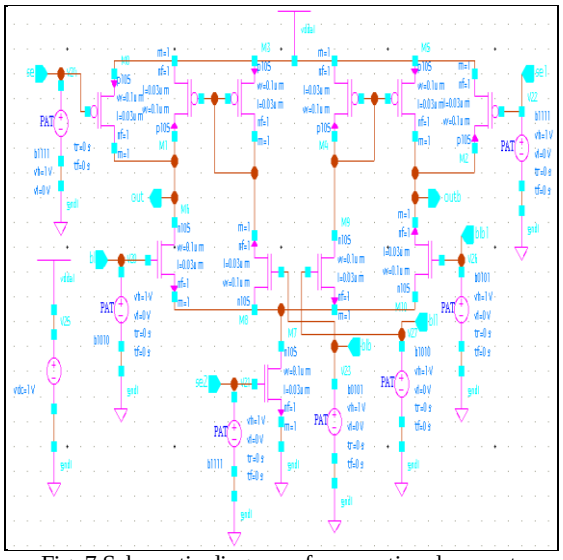

Fig. 7 Schematic diagram of conventional current mirror sense amplifier

Based on the values of control signals "cs", "se" and "seb", the sense amplifier operates in two modes precharge mode and sensing mode. During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M0 transistor is made ON by enabling the control signal "cs". During precharge mode other control signal "se" and "seb" are disabled. During sensing mode control signals "se" and "seb" are given values 1 and 0 so M3, M11 and M10 transistors are turned ON which allows supply voltage and ground terminal to get connected to the circuit. The transistors M6 and M9 are turned ON during sensing mode which allows inputs "bl" and "blb" to the sense amplifier. The sense amplifier senses the output based on the inputs "bl" and "blb".

2.6 Conventional Current Mirror Sense Amplifier (CCISA)

The CCISA consists of eleven transistors [2] in which two transistors are used to precharge the output nodes of sense amplifier and one transistor is enabled for sensing the data. The schematic diagram of CCISA is shown in Fig. 7

Based on the values of control signals "se", "se1" and "se2", the sense amplifier operates in two modes, precharge mode and sensing mode. During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M0 and M2 transistors are made ON by enabling the control signal "se" and "se1". During precharge mode the control signal "se2" is disabled. During sensing mode transistor M7 is made ON by enabling the control signal "se2" which allows ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb".

2.7 Cross Coupled Sense Amplifier (CCSA)

The CCSA consists of eight transistors in which one transistor is used to precharge the output nodes of sense amplifier and one transistor is enabled for sensing the data [9]. The schematic diagram of CCSA is shown in Fig. 8

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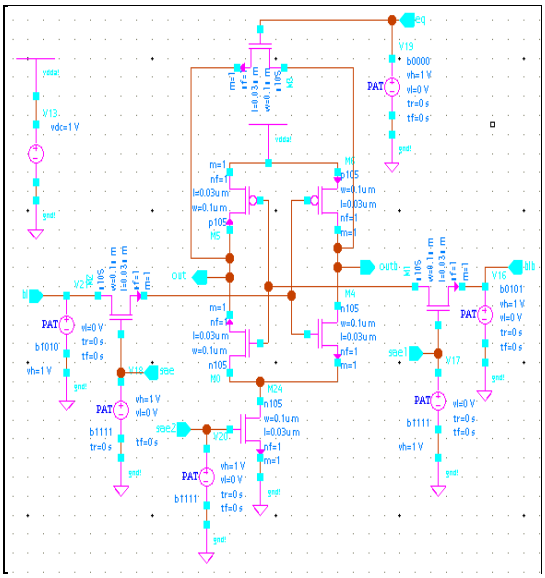

Fig. 8 Schematic diagram of cross coupled sense amplifier

The sense amplifier operates in two modes precharge mode and sensing mode based on the values of control signals "eq" and "sae". During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M3 transistor is made ON by enabling the control signal "eq". During precharge mode other control signal "sae" is disabled so inputs are available to the circuit only during sensing mode. During sensing mode control signals "eq" is disabled and "sae" is enabled so M1,M2 and M24 transistors are turned ON which allows inputs and ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb".

2.8 Hybrid Sense Amplifier (HSA)

The HSA consists of eleven transistors [11] in which one transistor is used to precharge the output nodes of sense amplifier and one transistor is enabled for sensing the data. The schematic diagram of HSA is shown in Fig. 9

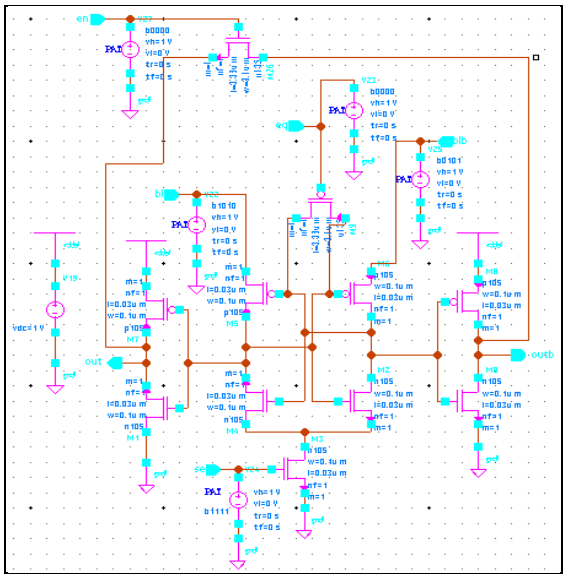

Fig. 9 Schematic diagram of hybrid sense amplifier

The sense amplifier operates in two modes precharge mode and sensing mode based on the values of control signals "en", "eq" and "se". During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M16 transistor is made ON by enabling the control signal "en". During precharge mode, control signal "eq" is disabled. The other control signal "se" is disabled during precharge mode so inputs are available to the circuit only during sensing mode. During sensing mode control signals "eq" is disabled and "se" is enabled so M9, M5, M6 and M3 transistors are turned ON which allows inputs and ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb".

2.9 Existing Sense Amplifier (ESA)

The ESA (proposed in the paper) consists of eleven transistors [9] in which one transistor is used to precharge the output nodes of sense amplifier and there is no transistor particularly enabled for sensing the data. The schematic diagram of ESA is shown in Fig. 10

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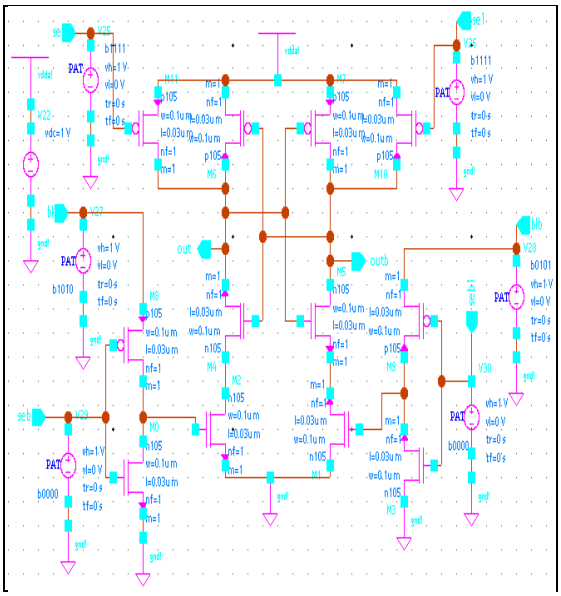

Fig. 10 Schematic diagram of existing sense amplifier

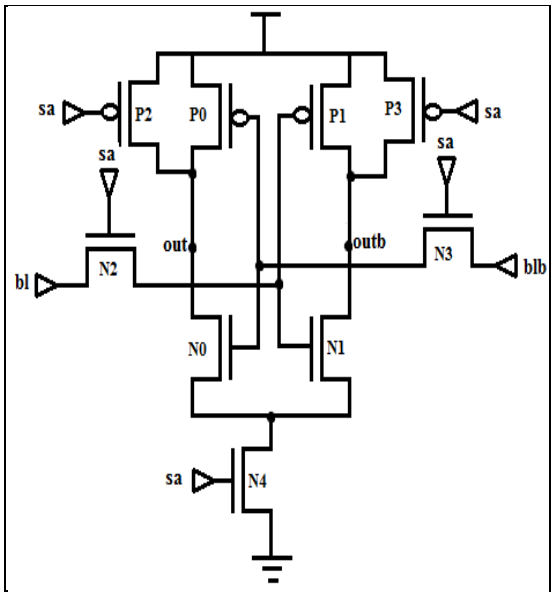

Fig. 11 Schematic diagram of proposed sense amplifier

The sense amplifier operates in two modes precharge mode and sensing mode based on the values of control signals "se", "se1", "seb" and "seb1". During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as M10 and M11 transistors are made ON by enabling the control signal "se" and "se1". During precharge mode, control signal "seb" and "seb1" is disabled so inputs are available to the circuit only during sensing mode. During sensing mode control signals "se" and "se1" are disabled and "seb" "seb1" are enabled so M8 and M9 transistors are turned ON which allows inputs and ground terminal to get connected to the circuit. The sense amplifier senses the output based on the inputs "bl" and "blb".

III. PROPOSED SENSE AMPLIFIER

The proposed sense amplifier consists of eleven transistors in which two transistors are used to precharge the output nodes of sense amplifier and one transistor is enabled for sensing the data. The schematic diagram proposed sense amplifier is shown in Fig.11

The sense amplifier operates in two modes precharge mode and sensing mode based on the value of control signal "sa". During precharge mode the output nodes "out" and "outb" are precharged to supply voltage level as P2 and P3 transistors are made ON by setting "sa" as zero. During sensing mode control signal "sa" is made as one so N2, N3, and N4 transistors are turned ON which allows inputs and ground terminal to get connected to the circuit. The main advantages of the sense amplifier is only one control signal is needed for the operation of the circuit and inputs are available to the circuit only during sensing mode. The sense amplifier senses the output based on the inputs "bl" and "blb".

IV. SIMULATION RESULTS AND GRAPHICAL ANALYSIS

A. Simulation result

The sense amplifiers are designed using SYNOPSYS (Custom designer) tool in 30nm technology. The parameters measured are dynamic power and delay [13]. The parameters power delay product, energy, energy delay product were calculated from measured values.

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Table I
Analysis of dynamic power dissipation for different sense amplifiers

Different Sense Amplifiers	Power dissipation in watts								
	0.6V	**0.7V**	**0.8V**	**0.9V**	**1V**	**1.1V**	**1.2V**	**1.3V**	**1.4V**
PFDSA	28.3n	35.6n	39.9n	61.2n	92.4n	143n	218n	338n	487n
LTSA	1.11u	1.66u	2.39u	6.38u	5.58u	8.25u	12.3u	17.6u	28.4u
CCMSA	69.3n	89.7n	113n	145n	216n	318n	447n	647n	959n
ALTSA	2.47u	4.13u	9.57u	15.5u	18.3u	32.2u	57.9u	107u	200u
DLSA	184n	198n	246n	318n	431n	485n	628n	702n	971n
CCMSA	613n	1.53u	3.02u	5.14u	7.88u	11.3u	15.3u	20u	25.4u
CCSA	36.8n	44.4n	55.2n	79.2n	113n	180n	286n	427n	614n
HSA	146n	466n	1.4u	3.04u	5.78u	9.77u	15.6u	23.2u	32.5u
Existing SA	11.1n	13.2n	16.5n	22n	28.9n	40n	59n	90.1n	137n
Proposed SA	35.5n	41.6n	50.8n	72.9n	111n	168n	260n	386n	548n

Table II
Analysis of energy dissipation for different sense amplifiers

Different Sense Amplifiers	Energy dissipation in Joule								
	0.6V	**0.7V**	**0.8V**	**0.9V**	**1V**	**1.1V**	**1.2V**	**1.3V**	**1.4V**
PFDSA	56.6n	71.2n	79.8n	122.4n	184n	286n	436n	676n	974n
LTSA	2.22u	3.32u	4.78u	12.76u	11.6u	16.5u	24.6u	35.2u	56.8u
CCMSA	138.6n	179.4n	226n	290n	432n	636n	894n	1294	1918n
ALTSA	4.94u	8.26u	19.4u	31u	36.6u	64.4u	115u	214u	400u
DLSA	368n	396n	492n	636n	862n	970n	1256n	1404n	1942n
CCMSA	1226n	3.06u	6.04u	10.28u	15.7u	22.6u	30.6u	40u	50.8u
CCSA	73.6n	88.8n	110n	158.4n	226n	360n	576n	854n	1228n
HSA	292n	932n	2.8u	6.08u	11.5u	19.54u	31.2u	46.4u	65u
Existing SA	22.2n	26.4n	33n	44n	57.8n	80n	118n	180n	274n
Proposed SA	71n	83.2n	101n	145.8n	22n	336n	520n	772n	1096n

Table I shows the power dissipation of different sense amplifiers which describes that if inputs are available during precharge mode, power dissipated will be more. The reason is more transistors will be in ON state including transistors which is made ON for precharging the output nodes. Table II shows the energy analysis for different sense amplifiers which describes that

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how much energy is dissipated by each sense amplifier during its operation.

B. Waveform result

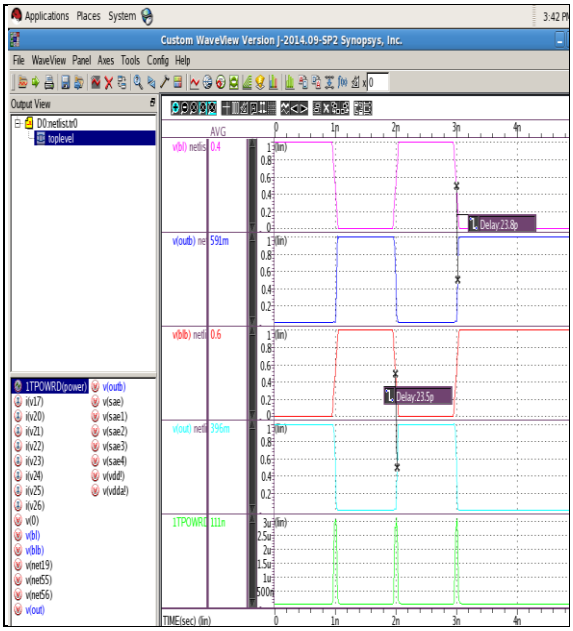

Fig. 12 Simulation result of proposed sense amplifier

Fig. 12 shows the simulation result of proposed sense amplifier. The waveforms in the figure indicate that when control signal "sa" is asserted to one the sense amplifier senses the outputs based on the inputs. The inputs are "bl" and "blb" and outputs are "out" and "outb". In the graph X-axis specifies time period and Y-axis specifies the voltage level.

C. Layout

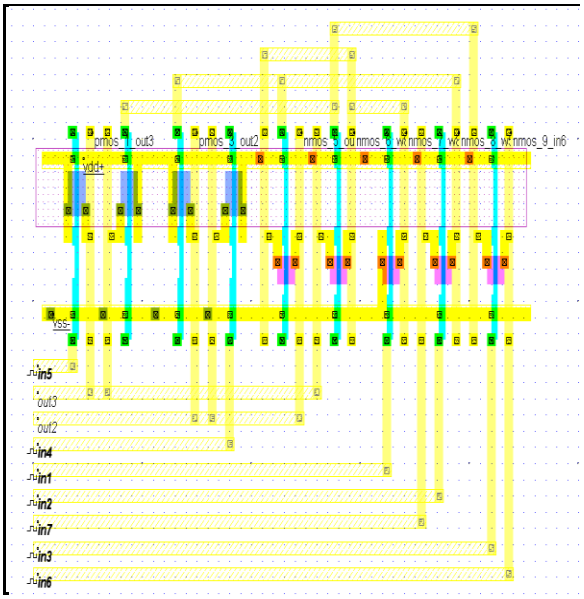

Fig. 13 Layout of proposed sense amplifier

The layout of proposed sense amplifier is shown in Fig.13. The layout of proposed sense amplifier cell is generated using Microwind tool. Although it causes some area overhead due to use of separate transistors for precharging and sensing the nodes, it is least concern in nanometer regime.

D. Graphical representation of different parameters for sense amplifier designs

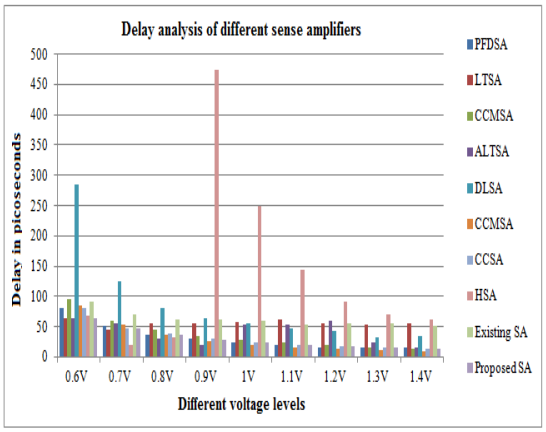

Fig. 14 Delay analysis of different sense amplifiers

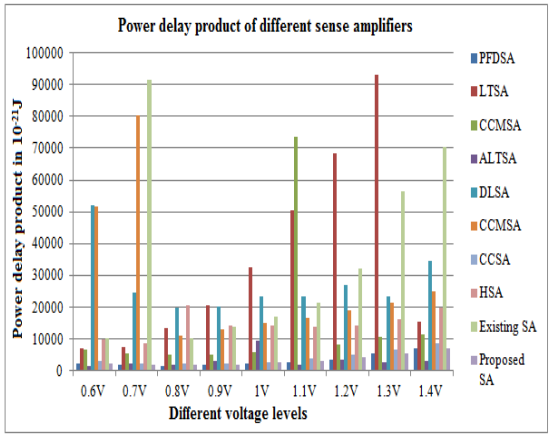

Fig. 15. Power delay product analysis of different sense amplifiers

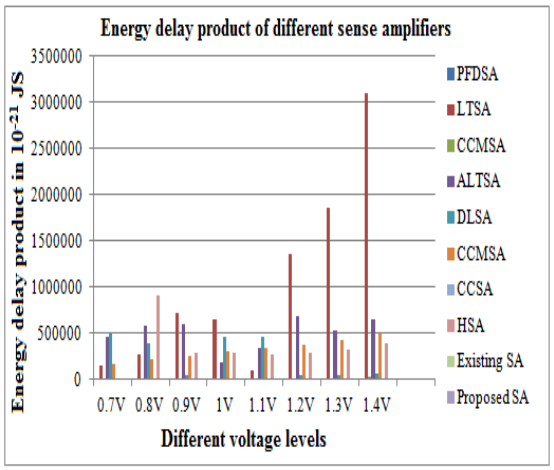

Fig. 16 Energy delay product analysis of different sense amplifiers

Fig. 14, Fig. 15, Fig. 16 shows delay, power delay product and energy delay product [13] analysis of different sense amplifiers in which proposed one provides better reduction than other sense amplifiers. The values of the proposed sense amplifier gets reduced due to its fast operation during sensing mode.

V. CONCLUSION

The sense amplifier in the memory array structure plays an important role in memory read operation. The main function of the sense amplifier is to sense the data, so sensing should be done fast to reduce the delay during read operation. The sense amplifier proposed provides better reduction in delay and power delay product though increase in little amount of power dissipation. As only one sense amplifier is used per column in the array structure, little increase in power dissipation is not taken into account. The proposed sense amplifier reduces the dynamic power dissipation, delay, power delay product, energy, energy delay product by 8%, 12%, 17%, 10% and 15% compared to cross coupled sense amplifier. Comparision of proposed is made over cross coupled sense amplifier because the operation of both remains same during the sensing mode, the difference occurs during precharge mode.The proposed sense amplifier can be used in memory array structure for fast memory read operation.

REFERENCES

[1] Shalini Singh, Shyam Akase, "Low Power Consuming 1 KB (32X32) Memory ArrayUsing Compact 7T SRAM Cell," Wireless Pers Commun, Springer, Vol.96, pp.1099-1109, 2017.

[2] H.Kang, S.O.Jung, "Offset - Cancelling Current- Sampling Sense Amplifier for Resistive Non Volatile Memory in 65nm CMOS," IEEE Journal of solid state circuits, Vol.52, 2017.

[3] Jeong.H, "Switching PMOS sense amplifier for high density low voltage single ended SRAM," IEEE Trans Circuits Syst, Vol.62, pp.1555-1563, 2016.

[4] Sandeep kumar, Charanjeet Singh, "Study of Voltage and Current Sense amplifier," International Journal of Recent trends in Engineering and Research,Vol2, 2016.

[5] Kim.J, Song.B, "Latch offset cancellation sense amplifier for deep submicrometer STT-RAM," IEEE Tran Circuit Syst, Vol.62, pp.1776-178, 2015.

[6] J.Kim, J.P.Kim, "A double sensing margin offset cancelling dual stage sensing circuit for resistive non volatile memory," IEEE Trans Circuit Syst, Vol.62, pp. 1109-1113, 2015.

[7] Kim.J, Song.B, "Latch offset cancellation sense amplifier for deep submicrometer STT-RAM," IEEE Tran Circuit Syst, Vol.62, pp.1776-1784, 2015.

[8] Meenu Rani Garg, Anu Tonk, "A study of different types of voltage and current sense amplifiers used in SRAM," International Journal of Advanced Research in Computer and Communication Engineering, Vol.4, 2015.

[9] Kamal Kant Joshi, Jyoti Kedia, "Performance analysis of sense amplifiers," International Journal of Advanced Engineering Research and Technology, Vol.3, 2015.

[10] Vivek.K,Hemaprabha.A, "Implementati -on of latch type sense amplifier," International Journal of Research in Engineering and Technology, Vol.3,2014.

[11] Patel.P, Soni.H, "Performance of various sense sense amplifier topologies in sub100nm Planar MOSFET technology," International Journal of Emerging Trends and Technology in Computer Science, Vol.3, pp.645-649, 2014.

[12] Hassan.M, Halim.A ,"Comparative study on 8T SRAM with different types of sense amplifier," International Conference on Semiconductor Electronics, 2014.

[13] Garg.A, Kim.T, "SRAM array structures for energy efficiency enhancement," IEEE Transactions on Circuits and System-II, Vol.60, pp. 351–355, 2013.
[14] Bellerimath, P.S, Banakar, R.M," Implementation of 16X16 SRAM memory array using 180 nm technology," International Journal of Current Engineering and Technology, Vol.4, pp.2277–4106, 2013.